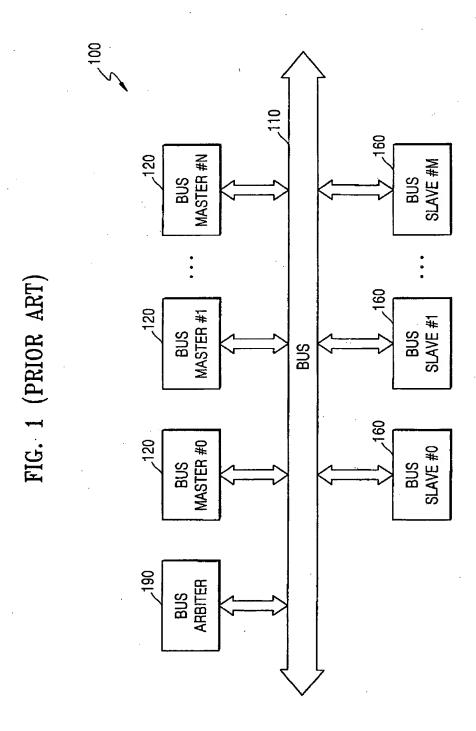
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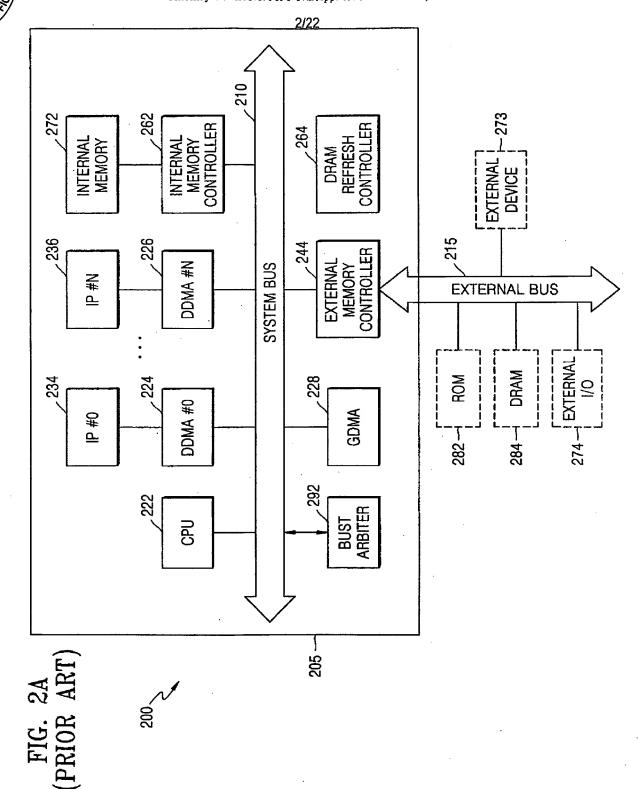
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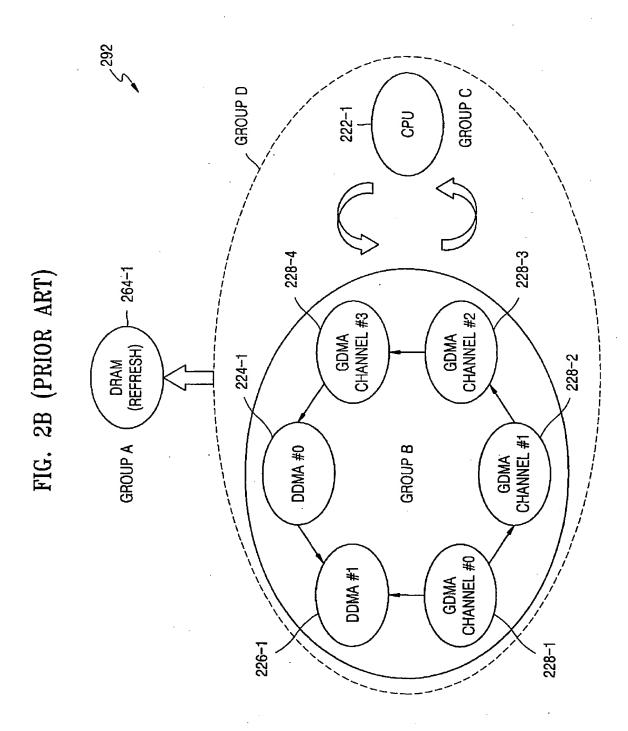
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PRIORIT ORDER	Y 프	WOJ	PF	riority Order —	HGH	
GDMA CHANNEL #2 GDMA CHANNEL #3 DDMA #0 DDMA #1 GDMA CHANNEL #0	STEP 5 FUNCTIONAL BLOCKS DRAM REFRESH CPU	GDMA CHANNEL #2 GDMA CHANNEL #3	GDMA CHANNEL #0 GDMA CHANNEL #1	DDMA #0 DDMA #1	FUNCTIONAL BLOCKS DRAM REFRESH	STEP 1
$\hat{\Omega}$				$\hat{\mathbf{U}}$		
PRIORIT ORDER		LOW -	—— PF	RIORITY — DRDER		_
DDMA #0 DDMA #1 GDMA CHANNEL #0 GDMA CHANNEL #1 CPU	STEP 6 FUNCTIONAL BLOCKS DRAM REFRESH BENANNEL #2	GDMA CHANNEL #3 CPU	GDMA CHANNEL #1 GDMA CHANNEL #2	DDMA #1 GDMA CHANNEL #0	FUNCTIONAL BLOCKS DRAM REFRESH	FIG. 2C (
Û				$\hat{\Omega}$		(PRIOR ART)
PRIORIT ORDER	Y 등	WO.	PF	riority Order —	High	OR.
	3 3 3 3					
DDMA #0 DDMA #1 GDMA CHANNEL #0 GDMA CHANNEL #1 GDMA CHANNEL #2	STEP 7 FUNCTIONAL BLOCKS DRAM REFRESH CPU	GDMA CHANNEL #3 DDMA #0	GDMA CHANNEL #1 GDMA CHANNEL #2	DDMA#1 #0	FUNCTIONAL BLOCKS DRAM REFRESH	ART) STEP 3
DDMA #0 DDMA #1 DDMA #1 GDMA CHANNEL #0 GDMA CHANNEL #2	STEP 7 FUNCTIONAL BLOCKS DRAM REFRESH CPU		GDMA CHANNEL #1 GDMA CHANNEL #2	GDMA CHANNEL #0	FUNCTIONAL BLOCKS DRAM REFRESH	ART) STEP 3
DDMA #0 DDMA #1 DDMA #1 GDMA CHANNEL #0 GDMA CHANNEL #1 GDMA CHANNEL #2 LOW			PF		FUNCTIONAL HIGH BLOCKS A DRAM REFRESH	ART) STEP 3

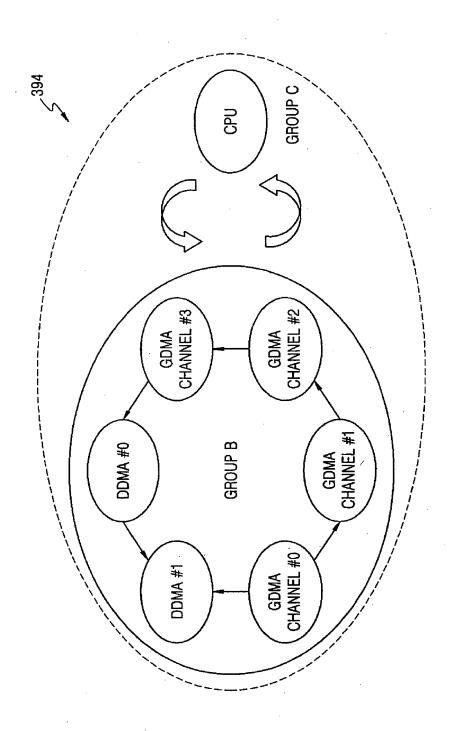
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5/22 210 273 CONTROLLER MEMORY MEMORY NTERNAI INTERNAL 315 EXTERNAL MEMORY CONTROLLER BUS DDMA #N ₹ **EXTERNAL BUS** SYSTEM <u>_</u> EXTERNAL 1/0 **BUS ARBITER** DRAM EXTERNAL 8 S DDMA #0 **GDMA** 9 <u>a.</u> 282 284 274 396 SYSTEM BUS ARBITER SP

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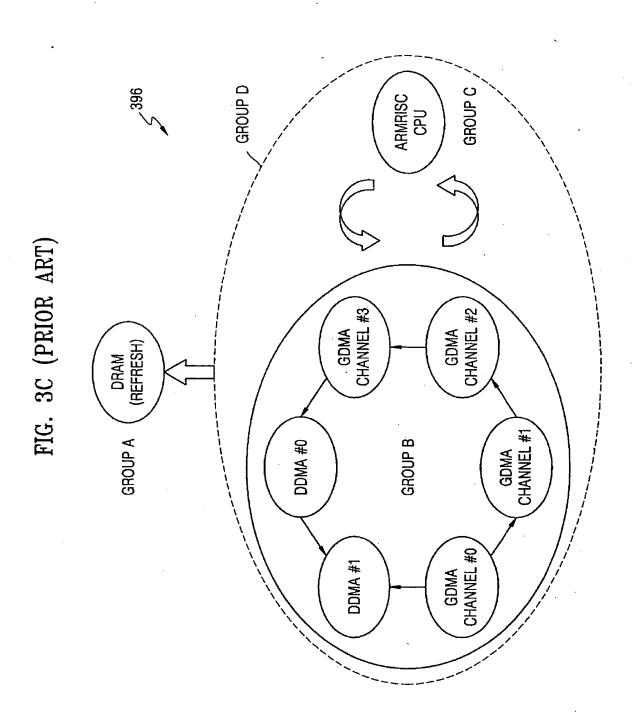
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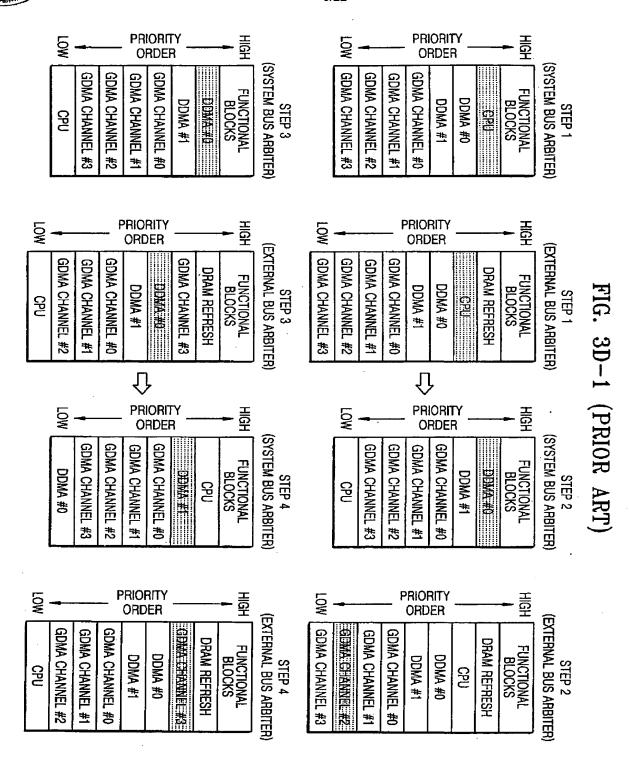




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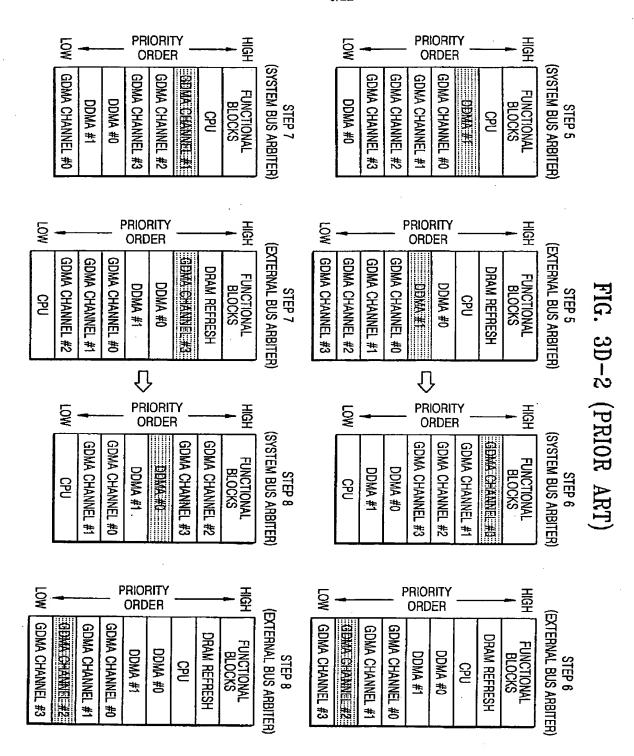


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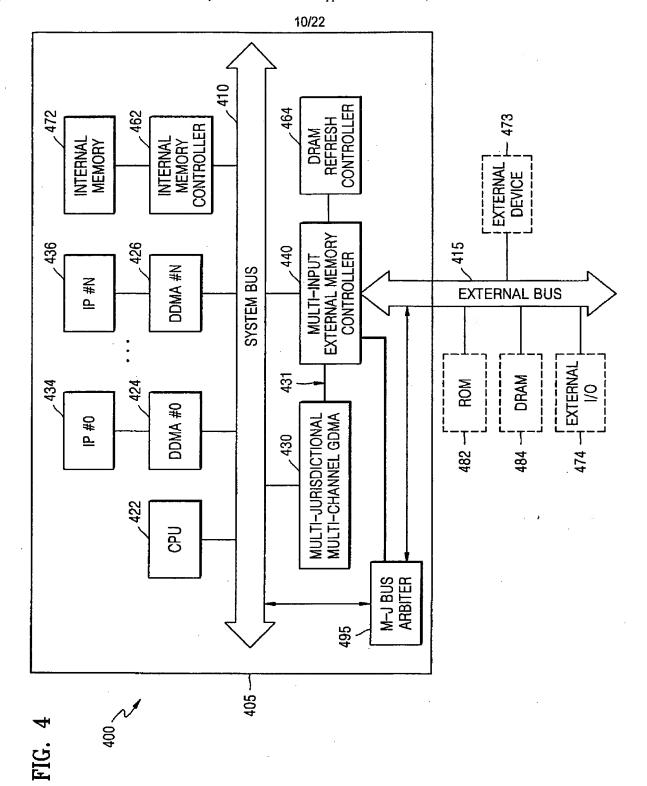
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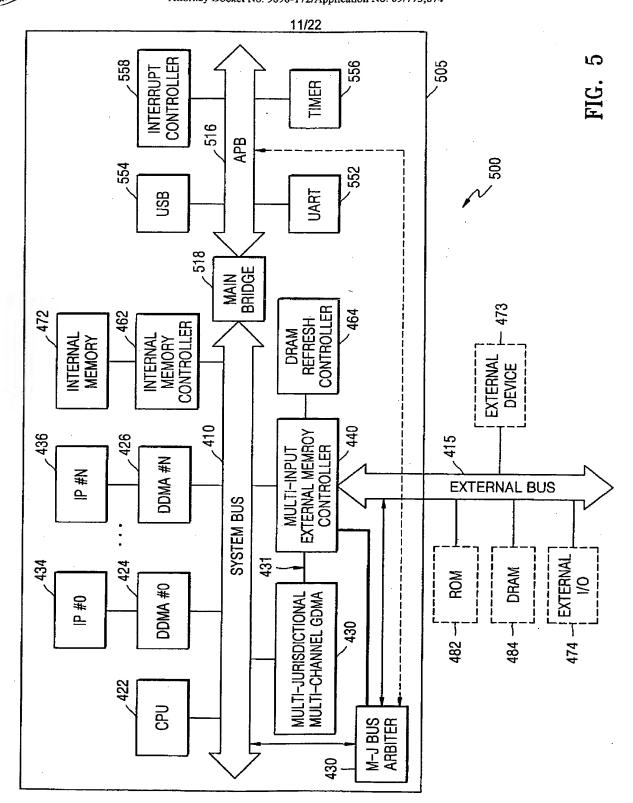


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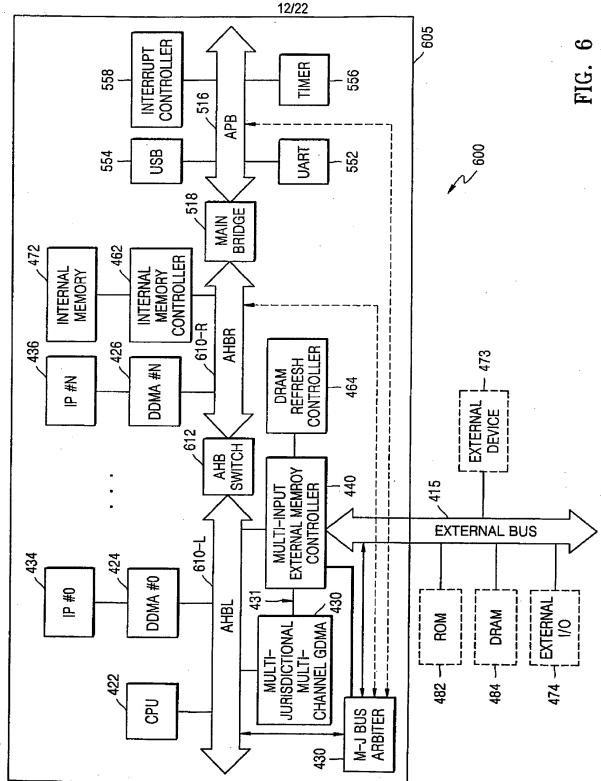


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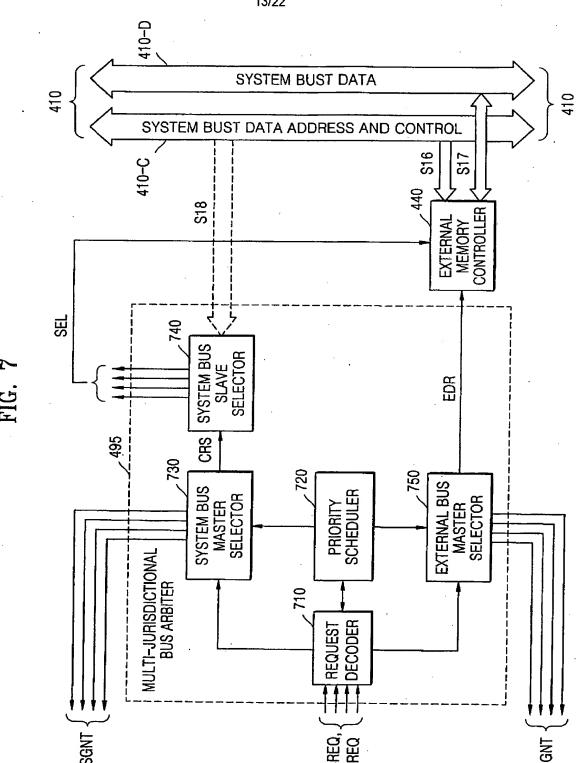


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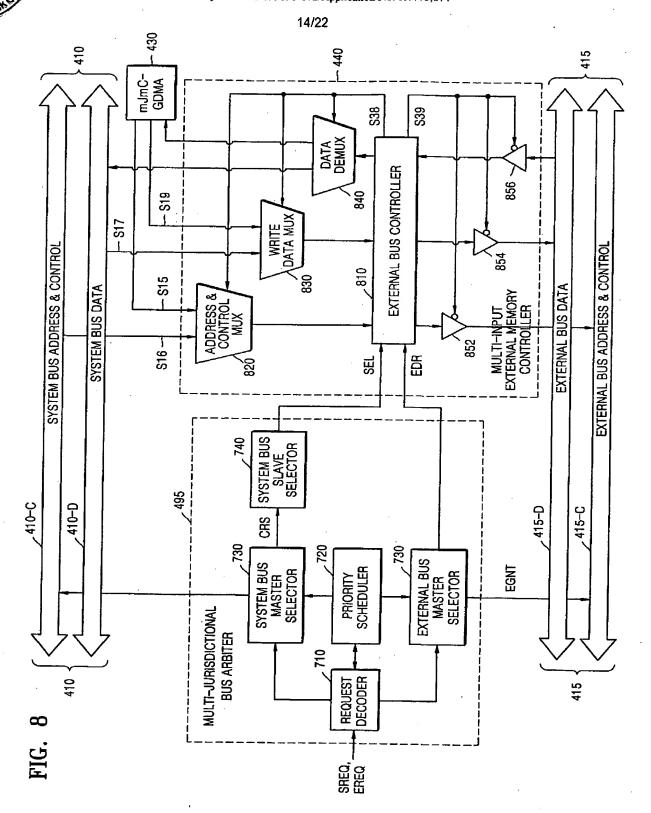


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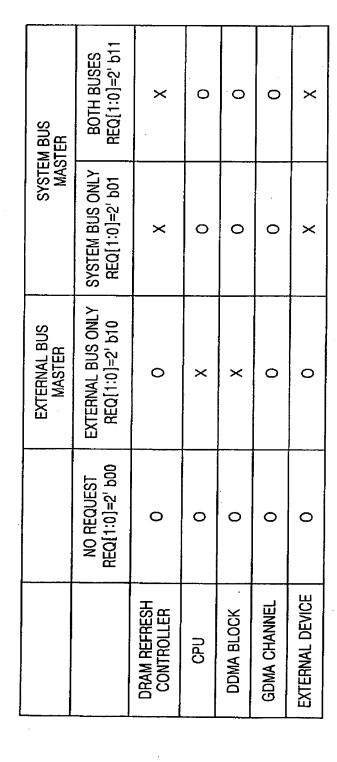
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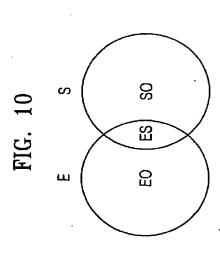
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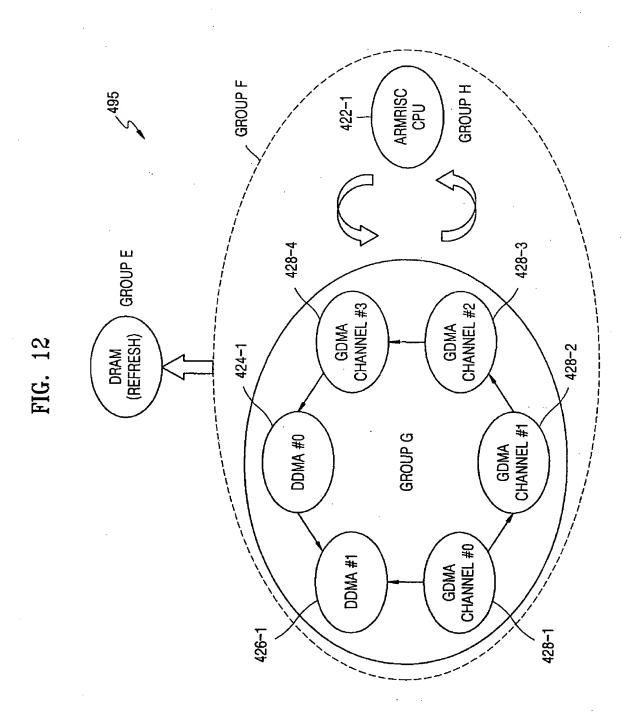
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FOR BOTH BUSES, SOFTWARE, AND METHOD FOR ASSIGNING PROGRAMMABLE PRIORITIES

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CLASSIFICATION OF SET	ELEMENT
SET OF FUNCTIONAL BLOCKS MAKING A SYSTEM BUS REQUEST (SYSTEM BUS MASTER S)	CPU, DDMA BLOCK, AND GDMA BLOCK
SET OF FUNCTIONAL BLOCKS MAKING AN EXTERNAL BUS REQUEST (E)	DRAM REFRESH CONTROLLER, CPU, DDMA BLOCK, GDMA CHANNEL, AND EXTERNAL DEVICE
SET OF FUNCTIONAL BLOCKS MAKING ONLY A SYSTEM BUS REQUEST (SO)	CPU
SET OF FUNCTIONAL BLOCKS MAKING ONLY AN EXTERNAL BUS REQUEST (EO)	DRAM REFRESH CONTROLLER, GDMA CHANNEL, AND EXTERNAL DEVICE
SET OF FUNCTIONAL BLOCKS MAKING A REQUEST FOR BOTH SYSTEM BUS AND EXTERNAL BUS (ES)	CPU, DDMA BLOCK, AND GDMA CHANNEL
SET OF FUNCTIONAL BLOCKS MAKING REQUESTS FOR A SYSTEM BUS OR AN EXTERNAL BUS (A)	DRAM REFRESH CONTROLLER, CPU, DDMA BLOCK, GDMA CHANNEL, AND EXTERNAL DEVICE

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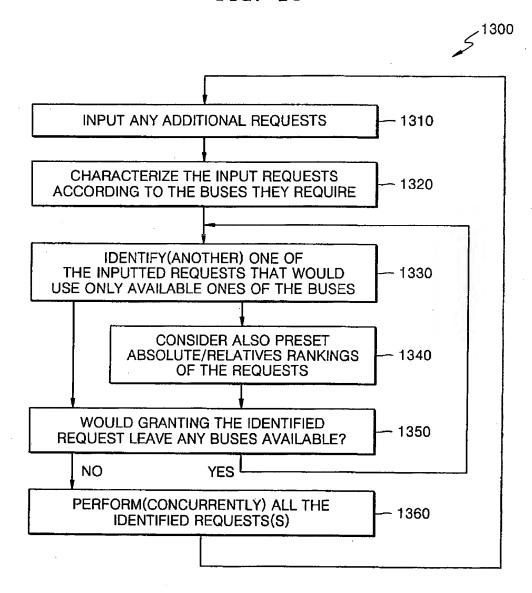
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FIG. 13



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SYSTEM ON A

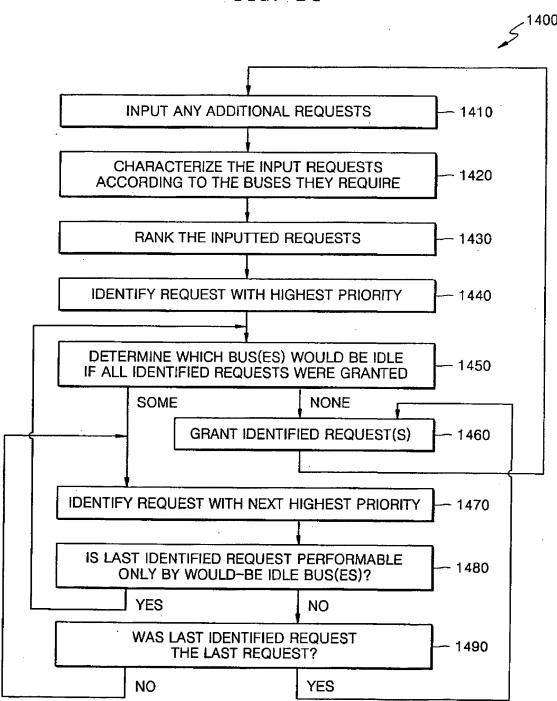
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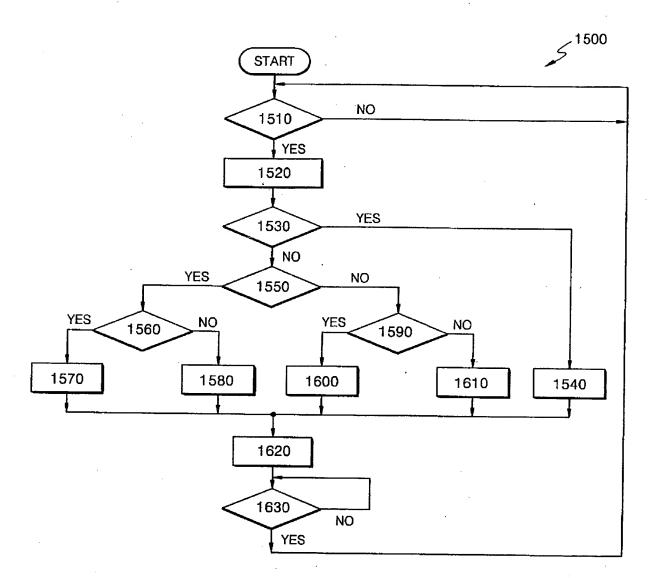
FIG. 14



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FIG. 15



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FOR BOTH BUSES, SOFTWARE, AND METHOD FOR ASSIGNING PROGRAMMABLE PRIORITIES Attorney Docket No. 9898-172/Application No. 09/773,874 21/22 PRIORITY PRIORITY 2 듄 **ORDER ORDER GDMA CHANNEL #1 GDMA CHANNEL #0 GDMA CHANNEL** THE DAMAGE AND Z# JANNYHO VMGB GDMA CHANNEL GDMA CHANNEL #1 GDMA CHANNEL DRAM REFRESH FUNCTIONAL BLOCKS DRAM REFRESH FUNCTIONAL BLOCKS DDMA #1 DDMA #0 DDMA #1 DDMA #0 1133 පි STEP STEP 1 . 35 . 悲 · ** 200 2'510 2'b11 2'611 2'500 2,000 2'b10 260 2,80 2511 2,01 贸 Ω **PRIORITY ₩** PRIORITY 플 포 **ORDER** ORDER **GDMA CHANNEL #3 GDMA CHANNEL** GDMA CHANNEL #2 GDMA CHANNEL #1 GDMA CHANNEL GDMA CHANNEL **GDMA CHANNEL** GDMA CHANNEL DRAM REFRESH FUNCTIONAL BLOCKS DRAM REFRESH FUNCTIONAL BLOCKS DOMA #0 DDMA #1 DWA#O DDMA #1 원 STEP 6 STEP 2 · ** #3 ** 杢 费 2 b0 2510 2'b10 2'00 2'600 2'510 2'b10 2^b1 2'501 2'51 贸 **PRIORITY** PRIORITY 쯢 Ş 팔 **ORDER ORDER** GDMA CHANNEL #3 GDMA CHANNEL #2 GDMA CHANNEL #0 GDMA CHANNEL #1 **GDMA CHANNEL GDMA CHANNEL** GDMA CHANNEL GDMA CHANNEL #0 FUNCTIONAL BLOCKS DRAM REFRESH FUNCTIONAL BLOCKS DRAM REFRESH DDMA 计划组 DDMA #0 TH WHEE STEP 7 윧 STEP 3 ** #3 #5 . <u>*</u> 2'510 2'b10 2'60 2'b01 2'b11 251 2'600 2510 2'b10 250 28 2 DT 贸 贾 $\hat{\Omega}$ **PRIORITY** PRIORITY 至 팚 8 **ORDER ORDER** GDMA CHANNEL #2 GDMA CHANNEL #3 GDMA CHANNEL OF STANKING WHOM EMACHANNEL #1 GDMA CHANNEL OF TANNANCO SYNCE DWA CHAWKE #2 DRAM REFRESH DRAM REFRESH FUNCTIONAL BLOCKS FUNCTIONAL BLOCKS DDMA DDMA DDMA #0

STEP

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22/22					
BUS UTILIZATION		n(EO)+2n(EO)+n(SO) 2n(A)	4n(SO)+3n(ES) 4n(S)		
VING BUS IATION	ELEMENT OF SET SO	1 n(A)	1 n(A)	n(EO)+n(SO) n(A)n(SO)	
Probability that element having bus Ownership performs operation	ELEMENT OF SET ES	1 n(A)	1 2n(S)	1 n(A)	
	ELEMENT OF SET EO	1 n(A)	n(ES)+2n(SO) 2n(S)n(EO)	n(EO)+n(SO) n(A)n(EO)	
ITEM		EXCLUSIVE BUS ARBITRATION	HIERACHICAL BUS ARBITRATION	PRESENT INVENTION	